20VL004 - FPGA Based System Design

Objective of the Course:

This course covers the advanced design and analysis of digital circuits with HDL. The primary goal is to provide in depth understanding of system design. The course enables students to apply their knowledge for the design of advanced digital hardware systems with help of FPGA tools.

1. Understand Digital system design using HDL.
2. Know FPGA architecture, interconnect and technologies.
3. Know different FPGA's and implementation methodologies.
4. Understand configuring and implementing digital embedded system, microcontrollers, microprocessors, DSP algorithm on FPGA.

Course Outcomes

Upon successful completion of this course, students will be able to:
1. Design and optimize complex combinational and sequential digital circuits
2. Model Combinational and sequential digital circuits by Verilog HDL
3. Design and model digital circuits with Verilog HDL at behavioural, structural, and RTL Levels
4. Develop test benches to simulate combinational and sequential circuits.
5. Understand the FPGA Architecture
6. Implementation of the combinational and sequential digital circuits in FPGA

UNIT I: Verilog HDL Coding Style: Lexical Conventions - Ports and Modules – Operators - Gate Level Modeling - System Tasks &Compiler Directives - Test Bench - Data Flow Modeling - Behavioral level Modeling -Tasks & Functions.

UNIT II:Overview of FPGA Architectures and Technologies:

FPGA Architectural options, coarse vs fine grained, vendor specific issues (emphasis on Xilinx FPGA), Antifuse, SRAM and EPROM based FPGAs, FPGA logic cells, interconnection network and I/O Pad.

UNIT III : Verilog Modelling of Combinational and Sequential Circuits: Behavioral, Data Flow and Structural Realization – Adders – Multipliers- Comparators - Flip Flops - Realization of Shift Register - Realization of a Counter- Synchronous and Asynchronous FIFO –Single port and Dual port RAM – Pseudo Random LFSR – Cyclic Redundancy Check.

UNIT IV Synchronous Sequential Circuit: State diagram-state table –state assignment-choice of flip-flops – Timing diagram –One hot encoding Mealy and Moore state machines – Design of serial adder using Mealy and Moore state machines - State minimization – Sequence detection- Design examples: Sequence detector, Serial adder, Vending machine using One Hot Controller.

UNIT V System Design Examples using Xillinx FPGAs – Traffic light Controller, Real Time Clock - Interfacing using FPGA: VGA, Keyboard, LCD, Embedded Processor Hardware Design.

References:

1. M.J.S. Smith, "Application Specific Integrated Circuits", Pearson, 2000.
2. Peter Ashenden, "Digital Design using VHDL", Elsevier, 2007.
3. Peter Ashenden, "Digital Design using Verilog", Elsevier, 2007. 4. W. Wolf, "FPGA based system design", Pearson, 2004.
4. Clive Maxfield, "The Design Warriors's Guide to FPGAs", Elsevier, 2004

5. Samir Palnitkar, “Verilog HDL: A Guide to Digital Design and Synthesis” Prentice Hall, Second Edition, 2003.
6. T.R. Padmanabhan, B.Bala Tripura Sundari, “Design through Verilog HDL” Wiley Interscience, 2004. S. Ramachandran, “Digital VLSI System Design: A Design Manual for implementation of Projects on FPGAs and ASICs Using Verilog” Springer Publication, 2007.
7. Wayne Wolf, “FPGA Based System Design”, Prentices Hall Modern Semiconductor Design Series.
8. Stephen Brown &ZvonkoVranesic, “Digital Logic Design with Verilog HDL” TATA McGraw Hill Ltd. 2nd Edition 2007.