20VL007 - VLSI TESTING & VALIDATION

Course Objectives:

- To involve the students in the theory and practice of VLSI test and validations.
- To introduce advanced techniques for efficiently testing and validating the VLSI design.
- To introduce the concept of Design for Test and the technique of automated test pattern generation.

Course Outcomes:

Upon successful completion of this course student should be able to:

CO1: To llustrate the logical and fault simulation techniques.

CO2: To effectively test VLSI systems using existing test methodologies, equipment's, and tools.

CO3: To Identify the methodology to test generation algorithms for combinational and sequential circuits.

CO3: To construct a Design for Testability (DFT) algorithm for VLSI Circuits.

CO4: To Summarizethedesignstrategiesfor test,systemlevelandmemorytest.

CO5: To ExplaintheconceptofBuiltInSelf-Testfordigitalsystems and itsmethodology.

CO6: To develop system level test

UNITI

BASICSOFTESTING:

NeedforTesting, TestingatVariousLevels,ObjectivesofTesting-VLSITestprocessandTest Equipment-TypesofTesting:FunctionalityTests,SiliconDebug,ManufacturingTests,Defectduring manufacturing - Fault Modelling, Observability and Controllability, Fault Coverage, Fault Sampling- ATE, Testeconomics.

UNITII

LOGICAL ANDFAULTSIMULATION:

Simulation for design verification, Simulation for Test evaluation - logical and fault simulation, CharacteristicsofFault Simulation,ClassicalFaultSimulationTechniques,ModernFaultSimulationfor CombinationalCircuits-HardwareApproachestoFaultSimulation.

UNITIII

COMBINATIONALANDSEQUENTIALCIRCUITSTESTGENERATION: Combinational Circuits: Algorithms representations, Redundancy Identification (RID), Significant CombinationalATPGAlgorithms,TestGeneration,TestCompaction-SequentialCircuits:ATPGfor singleclocksynchronouscircuits,Time-Frameexpansionmethod,Simulationbasedsequential circuits.

UNITIV

DESIGNSTRATEGIESFORTESTANDSYSTEMLEVELTEST:

DesignforTestability,AdhocTesting,ScanBasedTestTechniques,MemoryTesting,IDDQTesting, IDDQtestingMethods-BoundaryScan,BoundaryScanArchitecture,TestAccessPort(TAP),TAP Controller,InstructionRegisters,DataRegister,BoundaryScanRegister,BypassRegister.

UNITV

BUILT INSELFTEST:

BuitInSelfTest,TestPatternGenerationforBIST,CircularBIST,BISTArchitectures-TestableMemory Design,TestAlgorithms,TestGenerationforEmbeddedRAMs,BISTforDelayFaultTesting.

TextBooks

1. WesteandEshraghian,“PrinciplesofCMOSVLSIdesign”,PearsonEducation,1999.
2. M.L.BushnellandV.D.Agrawal,“EssentialsofElectronicTestingforDigital,Memoryand Mixed-SignalVLSICircuits”,KluwerAcademicPublishers,2004
3. P.K.Lala,“DigitalCircuitTestingandTestability”,AcademicPress,2002
4. N.K.JhaandS.G.Gupta,“TestingofDigitalSystems”,CambridgeUniversityPress,2003

Reference Books

1. W.W.Wen,“VLSITestPrinciplesandArchitecturesDesignforTestability”,Morgan Kaufmann.
2. A.L.Crouch,“DesignTestforDigitalIC’sandEmbeddedCoreSystems”,PrenticeHall International,2002.
3. ZainalabeNavabi,“DigitalSystemTestandTestableDesign:UsingHDLModelsand Architectures”, Springer,2010
4. A.KSharma,SemiconductorMemoriesTechnology,TestingandReliability,IEEE.
5. M.Abramovici,M.A.BreuerandA.D.Friedman,"DigitalSystemsandTestableDesign", Jaico PublishingHouse