20VL009 - PYTHON/TCL FOR SOFTWARE HARDWARE CO-DESIGN

Course Objectives:

1. Understand the Role of Scripting in VLSI Design.
2. Know Basics of Python and Tcl .
3. Know the HDL design libraries MyHDL and Pymtl.
4. Understand designing and implementation of combinational, Sequential circuits using Python, MyHDL and pymtl.

Course Outcomes

On completion of the course the Student is able to:

CO1: Design and Simulate Combinational Circuits.
CO2: Design and Simulate Finite State Machines (FSM).
CO3: Implementation of combinational circuits.
CO4: investigate the new designs for future development.

UNIT-1 : Basics of Tcl

UNIT-2 : Arrays and Data Handling and Plotting

Introduction to Python Language-Numbers, Strings, Lists, python control statements-if, for, range function, break and continue statements and else clauses on loops, pass statements, functions, data structures, input and output.

Introduction to Python Language-Numbers, Strings, Lists, python control statements-if, for, range function, break and continue statements and else clauses on loops, pass statements, functions, data structures, input and output. Numpy, pandas, Matplotlib.

UNIT-3

MyHDL-Introduction to MyHDL, Signals and concurrency, Parameters, ports and hierarchy: create a higher-level function with four instances of the lower-level functions

UNIT-4

PyMTL: Why PyMTL, The PyMTL Workflow, PyMTL basics which serve as the foundation for productive multi-level modeling and VLSI design, hardware implementation of a variant of Fletcher's checksum algorithm, Modeling Processors in PyMTL, Multi-Level Composition in PyMTL

UNIT-5

Case Study: AMBA BUS, Interacting with network devices,Digital Filter Blocks in MyHDL and their integration in pyFDA

Text Books:

1. http://www.myhdl.org/
2. J. Decaluwe. MyHDL: A Python-based Hardware Description Language. Linux journal, 2004(127):5, Nov. 2004.
3. Ieee standard for system verilog-unified hardware design, specification, and verification language. IEEE Std 1800-2012 (Revision of IEEE Std 1800-2009), pages 1--1315, Feb 013.
4. The MyHDL Manual. http://docs.myhdl.org/en/latest/manual/index.html, 2014.
5. Altera. Avalon interface specifications. http://www.altera.com/literature/manual/mnl_avalon_spec.pdf, 2014
6. https://github.com/xesscorp/myhdl-resources
7. https://www.fpgarelated.com/showarticle/25.php