# 20VL010 - Advanced Digital System Design

**Course Objectives**

To analyze synchronous and asynchronous sequential circuits

- To realize and design hazard free circuits
- To familiarize the practical issues of sequential circuit design
- To gain knowledge about different fault diagnosis and testing methods
- To estimate the performance of digital systems
- To know about timing analysis of memory and PLD

**Course Outcomes**

CO1: To Identify, design and analyse Synchronous and Asynchronous sequential logic circuits and design and develop system controller.
CO2: To learn and apply methods to analyse the timing behaviour and to detect timing hazards in digital circuits;
CO3: To Evaluate the digital system design by state identification techniques;
Co4: To analysis the methods for digital systems that incorporate programmable logic devices, RAMs
Co5: To examine the testing of combinational, sequential and PLAs design.
Co6: To develop PLA folding and minimization testing techniques.

**UNIT - I**

**SYNCHRONOUSSEQUENTIALCIRCUITDESIGN&ASMCHARTS:**ReductionofStateTablesStateAssignments, Sequential Circuit Design: - Design of Code Converter, Design of Iterative Circuits.Design of Sequential Circuits Using ROMs and PLAs, Sequential Circuit Design using CPLDs and FPGAs, ASMCharts.

**UNIT – II**

**ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN:** Analysis of Asynchronous Sequential Circuit (ASC) – Fundamental Mode Model, Flow Table, State Reduction, Design of ASC. Hazards, Races and Cycles.

**UNIT - III**

**STATE-IDENTIFICATION EXPERIMENTS AND TESTING OF SEQUENTIAL CIRCUITS:** Experiments, Homing Experiments, Distinguishing Experiments, Machine Identification, Checking Experiments, Design of Diagnosable Machines, Alternative Approaches to the Testing of Sequential Circuits, Built-In Self-Test (BIST).

**UNIT - IV**

**TIMING ANALYSIS:** ROM timings, Static RAM timing, Synchronous Static RAM and it's timing, Dynamic RAM timing, Complex Programmable Logic Devices, Logic Analyzer Basic Architecture, Internal structure, Data display, Setup and Control, Clocking and Sampling.

**UNIT – V**

**NEW GENERATION PROGRAMMABLE LOGIC DEVICES:** PLA Minimization and PLA Folding-The Compact Algorithm, Practical PLA s. PLA testing – Fault in PLA, Test Generation, DFT Schemes, Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000, Design Examples: ALU, barrel shifter, 4*4 Keyboard Scanner, multiplier

**TEXT BOOKS**


1. Charles H. Roth Jr. and Larry L. Kinney, "Fundamentals of Logic design", 6th ed.,Thomson Learning,2004.
2. Parag K Lala, "Digital Circuit Testing and Testability", Academic Press,2002.
3. ZviKohavi and Niraj K.Jha, "Switching and Finite Automata Theory",3rd., Cambridge University Press,2010.
4. Nripendra N Biswas, "Logic Design Theory", Prentice Hall of India,2001.
5. JohnMYarbrough,"DigitalLogicapplicationsandDesign",ThomsonLearning,2001.


REFERENCEBOOKS


1. Donald G. Givone, "Digital principles and Design", TataMcGraw Hill 2002.
2. Stephen Brown and ZvonkVranesic, "Fundamentals of Digital Logic with VHDLDeisgn", Tata McGraw Hill,2002.
3. Mark Zwolinski, "Digital System Design with VHDL", Pearson Education,2004.