20VL011 - VLSI SIGNAL PROCESSING

Course Objectives:
(i) To introduce efficient design of DSP architectures suitable for VLS
(ii) To introduce techniques for altering the existing DSP structures to suit VLSI implementations

Course Outcomes:
Upon successful completion of this course student should be able to:
CO1 :Compute the iteration bound of a circuit
CO2: Effectively to apply CRITICAL PATH REDUCTION techniques in VLSI architectures
CO3 :Perform pipelining and parallel processing in FIR systems to achieve high speed and low power
CO4: Improve the speed of digital system through transformation techniques.
CO5 :Apply systolic and bit level architectures to improve the efficiency of VLSI circuits
CO6 :Use of proper techniques for parallel processing design for scaling and roundoff noise computation.

UNIT I :Introduction
Introduction to DSP Systems: Introduction To DSP Systems -Typical DSP algorithms;
Iteration Bound – data flow graph representations, loop bound and iteration bound, Algorithms For Computing Iteration Bound, Iteration Bound of Multirate Data Flow Graphs; **Pipelining and parallel processing:** Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power

UNIT II : METHODS OF CRITICAL PATH REDUCTION
Retiming : Definitions and properties Retiming techniques; Solving systems of inequalities, Retiming Techniques. **Unfolding**: Algorithm for Unfolding, properties of unfolding, Critical path Unfolding and Retiming applications of Unfolding- sample period reduction and parallel processing application

UNIT – III: Systolic Architecture Design and Bit Level Arithmetic Architectures:
Systolic Architecture Design: Design methodology, FIR systolic arrays; **Bit Level Arithmetic Architectures**: Parallel Multipliers, Bit-Serial Multipliers, Bit-Serial Filter Design and Implementation, Canonic Signed Digit Arithmetic, Distributed Arithmetic.

UNIT-IV: ALGORITHMIC STRENGTH REDUCTION METHODS andRecursive filters Design
Fast Convolution: Fast convolution – Cook-Toom algorithm, modified Cook-Took algorithm – Wino grad Algorithm, Modified Wino grad Algorithm ;**Algorithmic strength reduction:** Algorithmic strength reduction in Filters-Parallel FIR Filters, DCT and Inverse DCT;**Pipelinedand Parallel Recursive filters Adaptive Filters:**– Pipelining in first- order IIR filters, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT – V: Scaling, Round off Noise and Numerical Strength Reduction
Scaling, Round off Noise: Scaling and Round off Noise- State variable Description of digital filters, Scaling and round off noise computation, Round off noise in pipelined I order IIR filters. **Numerical Strength Reduction**-Introduction, Sub expression Elimination, Multiple Constant Multiplication, Sub expression Sharing in Digital Filters, Additive and Multiplicative Number Splitting

REFERENCE BOOKS:

1. 1.Keshab K.Parhi, “VLSI Digital Signal Processing Systems, Design and Implementation”, John Wiley, Indian Reprint, 2007.
2. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Arrays", Springer, Second Edition, Indian Reprint, 2007.
3. S.Y.Kuang, H.J. White house, T. Kailath, “VLSI and Modern Signal Processing”, Prentice Hall, 1995.