20VL012 - LOW POWER VLSI Design

COURSE OBJECTIVE

To understand the critical requirements and implementation of Low-power VLSI circuits. The course also covers critical issue related to continuous scaling of microelectronic circuits.

COURSE OUTCOMES:

CO1: Acquires knowledge about the second order effects of MOS transistor characteristics.
CO2: Analyze various CMOS low power design techniques.
CO3: Apply low power design approaches to various logic circuits.
CO4: Learn in depth about power estimation techniques.
CO5: Design and implementation of computational structures for low power applications.
CO6: Analyze memories with efficient architectures to improve power.

UNIT - I

Fundamentals of Low Power VLSI Design: Need for Low Power Circuit Design
Sources of Power Dissipation: Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation
Short Channel Effects: Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT - II

For achieving low power: Switching activity reduction, algorithmic optimization, architecture optimization, logic optimization, circuit optimization.
Architectural Level Approach: Pipelining and Parallel Processing Approaches.
Different logic styles: Static and dynamic logic, Clock gating, reducing glitching through path balancing, input reordering.
Low-Power Design Approaches: VTCMOS circuits, MTCMOS circuits, Transistor stacking, power gating, Dynamic threshold CMOS.

UNIT - III

SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation. Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

UNIT - IV

Low-Voltage Low-Power Adders, Low-Voltage Low-Power Multipliers Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low- Voltage Low-Power Logic Styles.

UNIT - V

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Pre-charge and Equalization Circuit, Low Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. Kiat-Seng Yeo, Kaushik Roy, “Low-Voltage, Low-Power VLSI Subsystems”, TMH Professional Engineering.
2. Anantha P. Chandrakasan, and Robert W. Brodersen, Low Power Digital CMOS Design, Kluwer Academic Publications, 1995.

REFERENCE BOOKS:

1. Kaushik Roy, Sharat C. Prasad, "Low Power CMOS VLSI Circuit Design", John Wiley & Sons, 2000.
2. Gary K. Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Press, 2002.
3. Rabaey, and Pedram, Low Power Design Methodologies, Kluwer Academic,1997
4. Philip Allen, and Douglas Holberg, CMOS Analog Circuit Design, Oxford University Press, 2002.