20VL019 - SYSTEM ON-CHIP DESIGN

Course Objectives:

- To understand the concepts of System on Chip Design methodology for Logic and Analog Cores.
- To understand the concepts of System on Chip Design Validation.
- To understand the concepts of SOC Testing.

Course Outcomes

CO1: Upon successful completion of this course student should be able to: understand about SoC DesignMethodology.
CO2: Ability to understandthe design of different embeddedmemories.
CO3: Validation and Testing Concepts can beunderstood.
CO4: Investigate new techniques for future systems.

UNIT – I

Introduction- System tradeoffs and evolution of ASIC Technology- System on chip concepts and methodology – SoC design issues -SoC challenges and components.

UNIT – II

Design Methodological For Logic Cores- SoC Design Flow – On-chip buses –Design process for hard cores – Soft and firm cores – Core and SoC design examples.

UNIT – III

Design Methodology for Memory and Analog Cores- Embedded memories –Simulation modes Specification of analog circuits – A to D converter –Phase locked loops –High I/O.

UNIT – IV

Design Validation- Core level validation –Test benches –SoC design validation – Co simulation – hardware/ Software co-verification. Case Study: Validation and test of systems on chip.

UNIT – V

SoC Testing- SoC Test Issues –Cores with boundary scan –Test methodology for design reuse– Testing of microprocessor cores – Built in self-method –testing of embedded memories.

TEXT BOOKS:

1. RochitRajsunah,System-on-a-chip:DesignandTest,ArtechHouse,2007.
2. PrakashRaslinkar, Peter Paterson &Leena Singh, System-on-a-chip verification: Methodology and Techniques, Kluwer Academic Publishers,2000.

REFERENCE BOOKS:

1. M.Keating, D.Flynn, R.Aitken, A, GibbonsShi, Low Power Methodology Manual for System-on- Chip Design Series: Integrated Circuits and Systems, Springer,2007.
2. L.Balado,E.Lupon,Validationandtestofsystemsonchip,IEEEconferenceonASIC/SOC,1999.
3. A.Manzone, P.Bernardi, M.Grosso, M. Rebaudengo, E. Sanchez, M.SReorda, Centro Ricerche Fiat, Integrating BIST techniques for on-line SoC testing, IEEE Symposium on On-Line testing, 2000