(EC524) LOW POWER VLSI

Objective of the Course : *The goal of this course is to teach the students the principles of design, analysis, modeling and optimization of low power VLSI. This course covers the design of CMOS low power IC, approaches for power consumption estimation and methods of reducing switching & leakage power.*

UNIT-I

LOW POWER DESIGN, AN OVER VIEW: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator, MOS/BiCMOS PROCESSES: Bi CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

UNIT-II

LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of MOS/BiCMOS processes.

UNIT-III

DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations
of MOSFET models, Bipolar models, Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

UNIT-IV

CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and BiCMOS logic gates. Performance evaluation, LOW- VOLTAGE LOW POWER LOGIC CIRCUITS: Comparison of advanced BiCMOS Digital circuits, ESD-free Bi CMOS, Digital circuit operation and comparative Evaluation.

UNIT-V

LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip-flops, Design perspective.

TEXT BOOKS:

1. CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofail/ Gohl(3 Authors)-Pearson Education, Asia 1st Indian reprint,2002

REFERENCE BOOKS:

1. J.Rabaey, "Digital Integrated circuits", PH. N.J 1996

2. "sung-moKang and yusuf leblebici", CMOS Digital ICs, 3rd ed., TMH 2003(chapter11)

3. Parhi, :VLSI DSP systems", John Wiley & sons, 2003 (chapter 17)

4. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.